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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/960,089	09/21/2001	Michel Koopmans	4882US (01-0229)	5057

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TRASK BRITT
P.O. BOX 2550
SALT LAKE CITY, UT 84110

EXAMINER	
CHAMBLISS, ALONZO	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 01/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/960,089	KOOPMANS, MICHEL
	Examiner	Art Unit
	Alonzo Chambliss	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-97* is/are pending in the application.

4a) Of the above claim(s) *36-75 and 87-97* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24,29-35 and 76-86* is/are rejected.

7)☒ Claim(s) *25-28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Pre-amendment A filed on 11/20/01 has been fully considered and made of record in Paper No. 5.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-35 and 76-86, drawn to product, classified in class 257, subclass 777.

   II. Claims 36-75 and 87-97, drawn to process, classified in class 438, subclass 109.

3. The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the process as claimed can be used to make other and materially different product such as a product without designing the at least one redistribution circuit by forming a first dielectric layer made of polymer on the active surface, etching the first dielectric layer, and depositing a metal layer by sputtering the metal layer over the first dielectric.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Krista Powell on 4/3/02 a provisional election was made with or without traverse to prosecute the invention of product, claims 1-35 and 76-86. Therefore, claims 36-75 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention, since the attorney did not specify type of election. Affirmation of this election must be made by applicant in replying to this Office action.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Information Disclosure Statement

4. The information disclosure statement (IDS) submitted on 9/21/01 in Paper No. 2 was filed before the mailing date of the non-final rejection on 1/13/03. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

5. Figures 6-8 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction

or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

6. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: backside 74 page 11, line 23, backside 724 backside page 5 line 9,terminal pad 974' page 16 line 8, substrate 1030 page 16, line 12, and substrate 930''' page 15 line 5. Also, the drawings are objected to because they include the following reference sign(s) not mentioned in the description: 864, 921'', 924', 926, and 926'''. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

7. The drawings are objected to under 37 CFR 1.83(a) because they fail to show the combination of claims 22 and 23, the combination of claims 22-24, and the combination of claims 76-78 as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-3, 5-24, 21, 32-35, and 76-86, are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Yamada et al. (JP 6-132474).

With respect to Claims 1, 76, and 77, Yamada teaches a first semiconductor die 5c including an active surface and a backside, wherein the active surface including a plurality of bond pads 8c (i.e. located at the end of bump electrode 6c) and at least one redistribution bond pad circuit 10c, 11c (i.e. located the end of bump electrode 6b) at thereon. The plurality of bond pads 8c electrically connected to integrated circuitry of the first semiconductor die 5c. The at least one redistribution bond pad 11c circuit is independent from integrated circuitry of the first semiconductor die 5c and including a plurality of redistribution bond pads 11c. A second semiconductor die 5b includes an active surface, a backside, and a plurality of bond pads 8b (i.e. located the end of bump electrode 6a) on said active surface. The active surface of the second semiconductor die 5b faces the active surface of the first semiconductor die 5c. At least one electrical connector 6b extending between at least one bond pad 8b of the plurality of bond pads on the active surface of the second semiconductor die 5b and at least one redistribution bond pad of the plurality of redistribution bond pads 11c on the first semiconductor die 5c (see paragraph 11-21;Figs. 1 and 2a-2j).

With respect to Claims 2, Yamada teaches the first semiconductor die 5c is disposed on a substrate 3 (see Fig. 1).

With respect to Claim 3, Yamada teaches the first semiconductor die 5c electrically connected to the substrate 3 with intermediate conductive elements 6c (see Fig. 1).

With respect to Claim 5, Yamada teaches wherein the at least one redistribution bond pad circuit 10b, 11b comprises a plurality of conductive traces, wherein at least one conductive trace of the plurality of conductive traces connecting a first redistribution bond pad 11b of the plurality of redistribution bond pad 11b and a second redistribution bond pad 10b of the plurality of redistribution bond pads, the second redistribution bond pad 10b is proximate the perimeter of the first semiconductor die 5a (see Figs. 1 and 2a-2j).

With respect to Claim 6, Yamada teaches wherein the second 10b redistribution bond pad is electrically connected to the substrate 3 through semiconductor 5c (see Fig. 1).

With respect to Claim 7, Yamada teaches wherein peripheral edges of the first semiconductor die 5c and edges of the second semiconductor die 5b are substantially (i.e. almost equal to but not the same) vertically aligned (see Fig. 1).

With respect to Claim 8, Yamada teaches wherein the second semiconductor die 5b is smaller than the first semiconductor die 5c (see Fig. 1).

With respect to Claim 9, Yamada teaches wherein the at least one electrical connector 6b spaces the active surface of the second semiconductor die 5b from the active surface of the first semiconductor die 5c (see Fig. 1).

With respect to Claim 10, Yamada teaches a substrate 3 under the first semiconductor die 5c, wherein the substrate includes a plurality of contact areas thereon (see Fig. 1).

With respect to Claim 11, Yamada teaches wherein at least one bond pad of the plurality of bond pads 11c on the first semiconductor die 5c is electrically connected to a corresponding contact area of the plurality of contact areas on the substrate (see Fig. 1).

With respect to Claim 12, Yamada teaches wherein the at least one redistribution bond pad 11b is electrically connected to a corresponding contact area of the plurality of contact areas on the substrate 3 through the trace connected to the plurality of contact pads 11c (see Figs. 1 and 2c).

With respect to Claim 13, Yamada teaches at least one semiconductor die 5a vertically stacked on the substrate 3, wherein the backside of the first semiconductor 5c is located above the at least one stacked semiconductor die 5a (see Fig. 1).

With respect to Claims 14, 15, 34, and 35, Yamada teaches an insulative layer 9a (i.e. polymer resin adhesive material) between the first semiconductor die 5c and said second semiconductor die 5b (see paragraph 12;Figs. 2a-2e).

With respect to Claims 16, 17, 30, and 31, Yamada teaches wherein the at least one electrical connector 6b comprises a substantially a copper columnar pillar (see paragraph 25;Fig. 1).

With respect to Claims 19 and 20, any one of the semiconductor dies 5b or 5c can be viewed as either a first or second semiconductor die. Therefore, at least one peripheral edge of the second semiconductor die 5c extends laterally beyond at least one corresponding peripheral edge of the first semiconductor die 5b. Also, at least one electrical connector 6c extending from at least one bond pad of the plurality of bond pads 8c on the second semiconductor die 5c and a corresponding contact area of a substrate 3 (see Fig. 1).

With respect to Claim 21, Yamada teaches wherein at least one peripheral edge of the first semiconductor die 5c extends laterally beyond at least one corresponding peripheral edge of the second semiconductor die 5b (see Fig. 1).

With respect to Claim 22, Yamada teaches a substrate 3; a first semiconductor die 5b including an active surface, a second surface, and a plurality of peripheral edges, the second surface disposed on the substrate 3 by the semiconductor die 5c. The active surface has a plurality of bond pads 11b thereon. A second semiconductor die 5c includes an active surface, a second surface, a plurality of peripheral edges and a plurality of bond pads 11c on said active surface. The active surface of the second semiconductor die 5c faces the active surface of the first semiconductor die 5b while at least one edge of the plurality of peripheral edges of the second semiconductor die 5c extending laterally beyond at least one corresponding peripheral edge of said plurality of

peripheral edges of the first semiconductor die 5b. At least one connective element 6c extending from at least one bond pad 11c of the plurality of bond pads on said active surface of said second semiconductor die 5c to a corresponding contact area of the substrate 3 adjacent to the at least one corresponding peripheral edge of the first semiconductor die 5b (see Fig. 1).

With respect Claim 23, Yamada teaches at least one additional semiconductor die 5a stacked vertically between the first semiconductor die 5b and the second semiconductor die 5c (see Fig. 1).

With respect to Claim 24, Yamada teaches wherein the at least one additional semiconductor die 5a and the first semiconductor die 5b are all electrically connected to the substrate 3 by discrete conductive elements 6a which is electrically connected to the electrical connector 6c (see Fig. 1).

With respect to Claim 33, Yamada teaches wherein the at least one connective element 6c extends from the at least one bond pad 8c of the second semiconductor die 5c to the corresponding contact area of the substrate 3 (see Fig. 1).

With respect to Claim 79, Yamada teaches wherein the plurality of bond pads 8c is located proximate the perimeter of the active surface (see Fig. 1).

With respect to Claim 80, Yamada teaches wherein the at least one redistribution bond pad circuit 10c, 11c comprises a first redistribution bond 10c pad electrically connected to a second redistribution bond pad 11c (see Figs. 2a-2c).

With respect to Claims 81 and 82, Yamada teaches wherein the at least one redistribution bond pad circuit 10c, 11c further comprises a conductive trace made of

aluminum) extending between said first redistribution bond pad 11c and said second redistribution bond pad 10c (see paragraph 13; Figs. 2a-2e).

With respect to Claim 83, Yamada teaches wherein the first redistribution bond pad 11c is located on the active surface in a location that mirrors a location of a corresponding bond pad 8c of the second semiconductor device 5b to be positioned above the first semiconductor device 5c.

With respect to Claim 84, Yamada teaches wherein the second redistribution bond pad 10c is proximate the perimeter of the semiconductor device 5c (see Fig. 1).

With respect to Claim 85, Yamada teaches wherein the first redistribution bond pad 11c is electrically connected to a corresponding bond pad 8b on an active surface of a second semiconductor device 5b (see Fig. 1 and 2a-2e).

With respect to Claim 86, Yamada teaches wherein the second redistribution bond pad 10c is electrically connected to a contact area on a substrate 3 (see Fig. 1).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 4, 29, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. (JP 6-132474) as applied to claims 1, 3, 22, and 24 above, and further in view of Nguyen et al. (U.S. 6,238,949).

With respect to Claims 4 and 29, Yamada fails to disclose an intermediate conductive elements comprising of bonding wires. However, it is well known in the art to substitute bonding wires to electrically connected a semiconductor die to a substrate as evident by the prior art of Nguyen.

With respect to Claim 32, Yamada fails to disclose at least one connective element comprises a solder ball. However, Nguyen discloses at least one connective element comprises a solder ball 522. Therefore, it would have been obvious to substitute the solder ball for the bump electrode taught by Yamada, since the solder ball would provide a stable electrical connection between the primary die and the substrate as taught by Nguyen.

Allowable Subject Matter

12. Claims 25-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record does not teach or suggest the combination of a third semiconductor die of the at least one additional semiconductor die is disposed directly below the second semiconductor die. The third semiconductor die includes an active surface and a backside, wherein the active surface includes a plurality of bond pads 8apad circuit thereon, wherein the plurality of bond pads of said third semiconductor die electrically connected to integrated circuitry of said third semiconductor die, said at least

one redistribution bond pad circuit independent from the integrated circuitry of said third semiconductor die and including a plurality of redistribution bond pads.

The prior art made of record and not relied upon is cited primarily to show the process of the instant invention.

Conclusion

13. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (703) 306-9143. The fax phone number for this Group is (703) 308-7722 or 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956.

Alonzo Chambliss
Examiner
Art Unit 2827

AC/January 13, 2003